# ELEC 374 Phase 1 Report

Printouts of your Schematic

HDL codes

Printout of your testbenches

Functional simulation runs for all the tests

3.a) In the lab, demonstrate that your Logical AND circuitry works correctly by simulating the Control Sequence for the logical and R1, R2, R3 instruction (similar to table 4.7 on page 155 of the Lab Reader for the “add” instruction), modified for the Datapath in isolation, as follows:

Control Sequence:

Step Control Sequence

T0 PCout, MARin, IncPC, Zin

T1 Zlowout, PCin, Read, Mdatain[31..0], MDRin

T2 MDRout, IRin

T3 R2out, Yin

T4 R3out, AND, Zin

T5 Zlowout, R1in

3.b) Demonstrate that your Logical OR design works fine by simulating the Control Sequence for the or R1, R2, R3 instruction. The Control Sequence is the same as the one for the and instruction except for using the OR control signal in T4 instead of the AND signal.

3.c) Demonstrate that your Adder works correctly by simulating the Control Sequence for the add R0, R4, R5 instruction, modified for the Datapath in isolation, as follows:

Control Sequence:

Step Control Sequence

T0 PCout, MARin, IncPC, Zin

T1 Zlowout, PCin, Read, Mdatain[31..0], MDRin

T2 MDRout, IRin

T3 R4out, Yin

T4 R5out, ADD, Zin

T5 Zlowout, R0in

3.d) Demonstrate that your Subtract circuitry works fine by simulating the Control Sequence for the sub R0, R4, R5 instruction. The Control Sequence is the same as the one used for the add instruction except for using the SUB control signal in T4 instead of the ADD signal.

3.e) Demonstrate that your Multiplication circuitry works correctly by simulating the Control Sequence for the mul R6, R7 instruction.

Control Sequence:

Step Control Sequence

T0 PCout, MARin, IncPC, Zin

T1 Zlowout, PCin, Read, Mdatain[31..0], MDRin

T2 MDRout, IRin

T3 R6out, Yin

T4 R7out, MUL, Zin

T5 Zlowout, Loin

T6 Zhighout, HIin

You may need to use control signals to wait for the completion of the multiplication operation.

3.f) Demonstrate that your Division circuitry works fine by simulating the Control Sequence for the div R6, R7 instruction. The Control Sequence is similar to the mul instruction except for using the DIV control signal in T4 instead of the MUL signal. Be careful where the quotient and remainder are loaded inside the Z register, and change T5 and T6 control signals accordingly.

3.g) Demonstrate that your Shift Right circuitry works correctly by simulating the Control Sequence for the shr R1, R3, R5 instruction. The following Control Sequence is for a one-time shift right operation. Revise it accordingly for the count in R5.

Control Sequence:

Step Control Sequence

T0 PCout, MARin, IncPC, Zin

T1 Zlowout, PCin, Read, Mdatain[31..0], MDRin

T2 MDRout, IRin

T3 R3out, Yin

T4 SHR, Zin

T5 Zlowout, R2in

3.h) Demonstrate that your Shift Right Arithmetic circuitry works fine by simulating the Control Sequence for the shra R1, R3, R5 instruction. The Control Sequence is the same as the shr instruction except for using the SHRA control signal in T4 instead of SHR.

3.i) Demonstrate that your Shift Left circuitry works fine by simulating the Control Sequence for the shl R1, R3, R5 instruction. The Control Sequence is the same as the shr instruction except for using the SHL control signal in T4 instead of SHR.

3.j) Demonstrate that your Rotate Right circuitry works fine by simulating the Control Sequence for the ror R6, R6, R4 instruction. The following Control Sequence is for a one-time rotate right operation. Revise it accordingly for the count in R3.

Control Sequence:

Step Control Sequence

T0 PCout, MARin, IncPC, Zin

T1 Zlowout, PCin, Read, Mdatain[31..0], MDRin

T2 MDRout, IRin

T3 R6out, Yin

T4 ROR, Zin

T5 Zlowout, R6in

3.k) Demonstrate that your Rotate left circuitry works correctly by simulating the Control Sequence for the rol R6, R6, R4 instruction. The Control Sequence is the same as the ror instruction except for using the ROL control signal in T4 instead of ROR.

3.l) Demonstrate that your Negate circuitry works correctly by simulating the Control Sequence for the neg R0, R1 instruction.

Control Sequence:

Step Control Sequence

T0 PCout, MARin, IncPC, Zin

T1 Zlowout, PCin, Read, Mdatain[31..0], MDRin

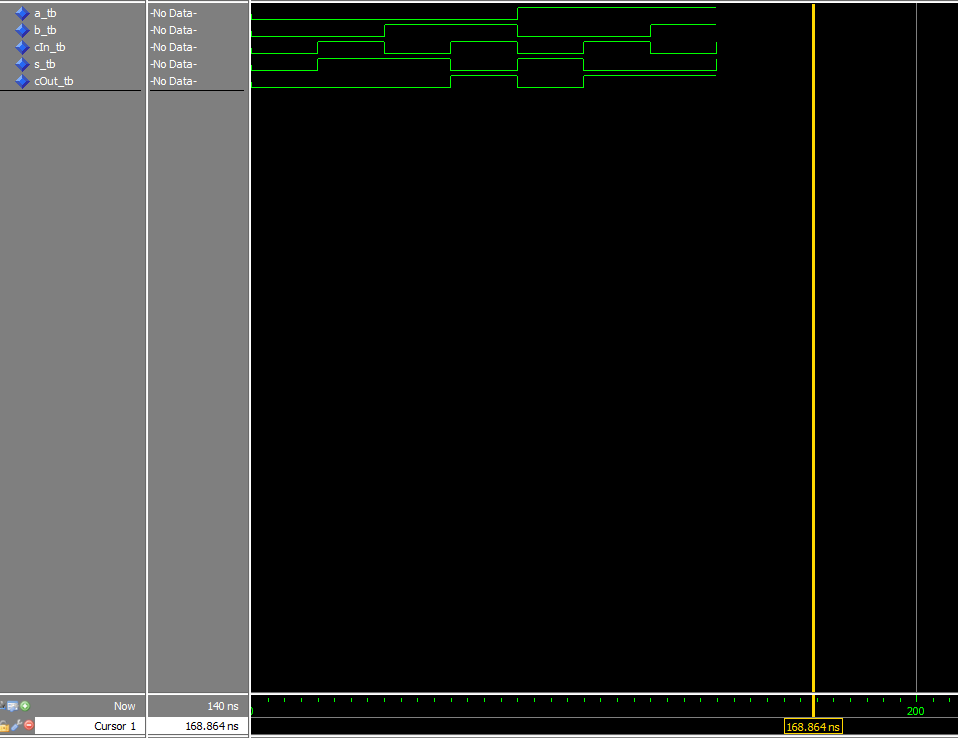
T2 MDRout, IRin

T3 R1out, NEG, Zin

T5 Zlowout, R2in

3.m) Demonstrate that your Not circuitry works correctly by simulating the Control Sequence for the not R0, R1 instruction. The Control Sequence is the same as the neg instruction except for using the NOT control signal in T3 instead of NEG. 3. Report: The phase 1 report (one per group) include: Printouts of your Schematic, HDL codes Printout of your testbenches Functional simulation runs for all the tests

# Full Adder



The full adder used here has three inputs, one being a carry. All eight possible values and their outputs are represented in this graph.